Sl No	Particulars		
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3	PhD Thesis Title	Design and Optimization of Multiply Accumulate and Comparator Units Based on Reversible Logic	
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7	Brief synopsis In recent years, the power dissipation is becoming important as packaging density increases in Complementary Metal-Oxide-Semiconductor circuits. Power reduction is the key parameter in low power designing of portable computing and sophisticated communication equipments. Various power optimization methods are available for the system designer at different abstraction levels namely device level, circuit/logic level, architecture level, algorithmic level and system level. One such method at circuit/logic level is reversible logic which is based on energy recovery method. Conventional circuits are irreversible circuits which dissipate power. Reversible circuits based on reversible logic do not dissipate power. Reversible logic is an emerging research area and a promising computing paradigm offering the main benefit of theoretically zero power dissipation. Reversible logic circuits and systems are popular now-a-days due to low power consumption and have applications in futuristic computing technologies like quantum computing, quantum cellular automata, DNA computing, optical computing, low power CMOS-VLSI, nanotechnology etc. This research work includes the design and synthesis of eight-bit reversible parallel binary adder/subtractor, the reversible binary multiplier to multiply two 4-bit numbers, the reversible sequential circuits such as reversible D-latch, D-flip-flop and shift register and the design of reversible n-bit binary comparator to compare two n-bit binary numbers. Integrating these components, the reversible Multiply-Accumulate unit is constructed.		